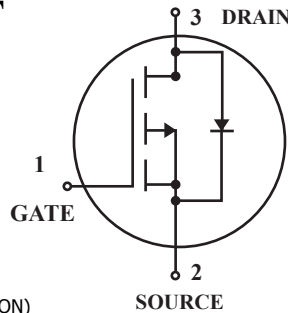


Surface Mount P-Channel Enhancement Mode MOSFET

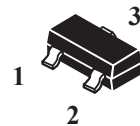
(Pb) Lead(Pb)-Free



DRAIN CURRENT
-550m AMPERES
DRAIN SOURCE VOLTAGE
-20 VOLTAGE

Features:

- *Super High Dense Cell Design For Low $R_{DS(ON)}$
 $R_{DS(ON)} < 600m\Omega @ V_{GS} = -10V$
- *Simple Gate Drive
- *Small package Outline
- *Fast Switching Speed
- *SOT-23 Package



SOT-23

Description

- *Designer with best combination of fast switching
- *Low on-resistance
- *Cost-effectiveness

Maximum Ratings ($T_A = 25^\circ C$ Unless Otherwise Specified)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ³ , ($T_A = 25^\circ C$) , ($T_A = 70^\circ C$)	I_D	-550	mA
		-440	
Pulsed Drain Current ^{1,2}	I_{DM}	2.5	
Total Power Dissipation ($T_A = 25^\circ C$)	P_D	1.0	W
Maximum Thermal Resistace Junction-ambient	$R_{\theta JA}$	125	$^\circ C/W$
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55~+150	$^\circ C$

Device Marking

WTC1333=1333

Electrical Characteristics ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Static

Drain-Source Breakdown Voltage $V_{GS}=0, I_D=-250\mu\text{A}$	BV_{DSS}	-20	-	-	V
Gate-Source Threshold Voltage $V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	$V_{GS(Th)}$	-0.5	-	-1.2	
Gate-Source Leakage current $V_{GS}=\pm 12\text{V}$	I_{GSS}	-	-	± 100	nA
Drain-Source Leakage Current ($T_j=25^\circ\text{C}$) $V_{DS}=-20\text{V}, V_{GS}=0$	I_{DSS}	-	-	-1	μA
Drain-Source Leakage Current ($T_j=70^\circ\text{C}$) $V_{DS}=-16\text{V}, V_{GS}=0$		-	-	-10	
Drain-Source On-Resistance $V_{GS}=-10\text{V}, I_D=-550\text{mA}$ $V_{GS}=-4.5\text{V}, I_D=-500\text{mA}$ $V_{GS}=-2.5\text{V}, I_D=-300\text{mA}$	$R_{DS(on)}$	-	-	600 800 1000	$\text{m}\Omega$
Forward Transconductance $V_{DS}=-5\text{V}, I_D=-550\text{mA}$	g_{fs}	-	1	-	S

Dynamic

Input Capacitance $V_{GS}=0\text{V}, V_{DS}=-10\text{V}, f=1.0\text{MHz}$	C_{iss}	-	66	105.6	pF
Output Capacitance $V_{GS}=0\text{V}, V_{DS}=-10\text{V}, f=1.0\text{MHz}$	C_{oss}	-	25	-	
Reverse Transfer Capacitance $V_{GS}=0\text{V}, V_{DS}=-10\text{V}, f=1.0\text{MHz}$	C_{rss}	-	20	-	

Switching

Turn-on Delay Time ² $V_{DS}=-10V, V_{GS}=-5V, I_D=-500mA, R_D=20\Omega, R_G=3.3\Omega$	$t_{d(on)}$	-	5	-	ns
Rise Time $V_{DS}=-10V, V_{GS}=-5V, I_D=-500mA, R_D=20\Omega, R_G=3.3\Omega$	t_r	-	8	-	
Turn-off Delay Time $V_{DS}=-10V, V_{GS}=-5V, I_D=-500mA, R_D=20\Omega, R_G=3.3\Omega$	$t_{d(off)}$	-	10	-	
Fall Time $V_{DS}=-10V, V_{GS}=-5V, I_D=-500mA, R_D=20\Omega, R_G=3.3\Omega$	t_f	-	2	-	
Total Gate Charge ² $V_{DS}=-16V, V_{GS}=-4.5V, I_D=-500mA$	Q_g	-	1.7	2.7	nC
Gate-Source Charge $V_{DS}=-16V, V_{GS}=-4.5V, I_D=-500mA$	Q_{gs}	-	0.3	-	
Gate-Source Change $V_{DS}=-16V, V_{GS}=-4.5V, I_D=-500mA$	Q_{gd}	-	0.4	-	

Source-Drain Diode Characteristics

Forward On Voltage ² $V_{GS}=0V, I_S=-300mA$	V_{SD}	-	-	-12	V
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- Note: 1. Pulse width limited by Max, junction temperature.
 2. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
 3. Surface mounted on FR4 board, $t \leq 10sec$.

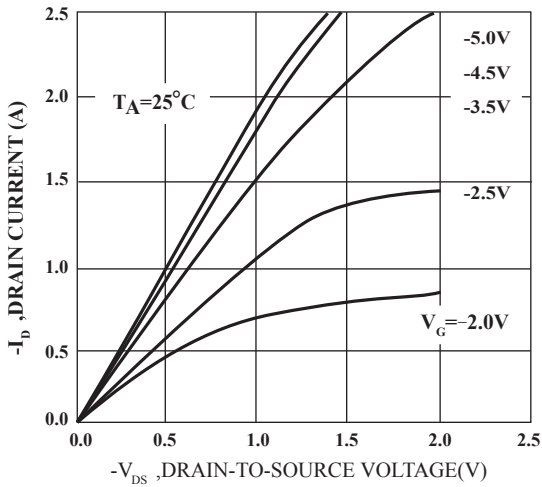


FIG.1 Typical Output Characteristics

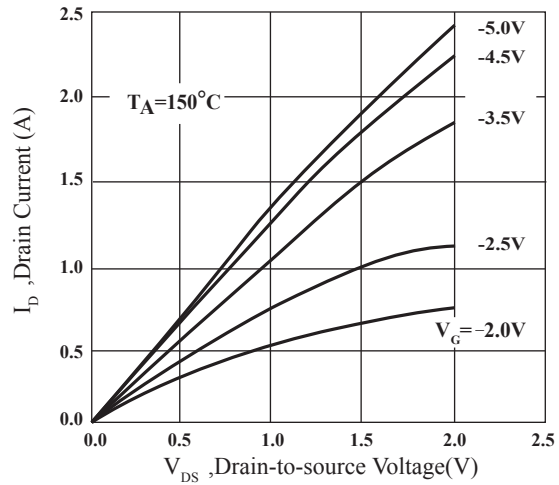


Fig.2 Typical Output Characteristics

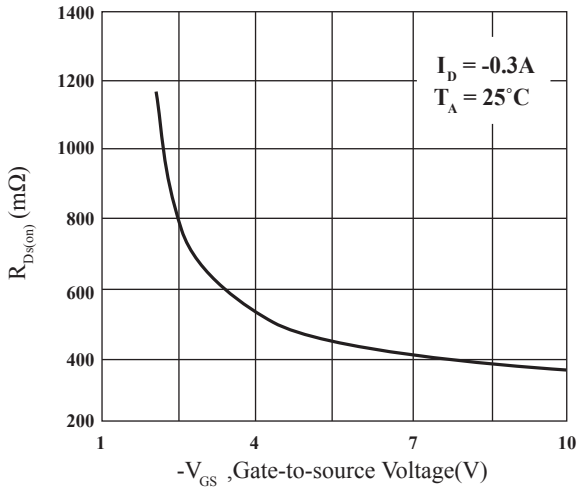


Fig.3 On-Resistance v.s. Gate Voltage

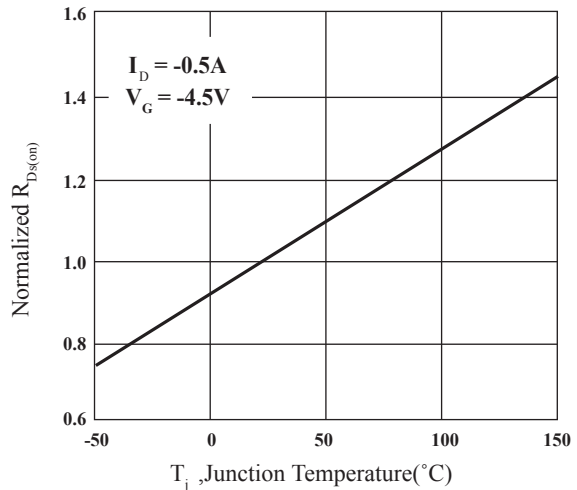


Fig.4 Normalized OnResistance

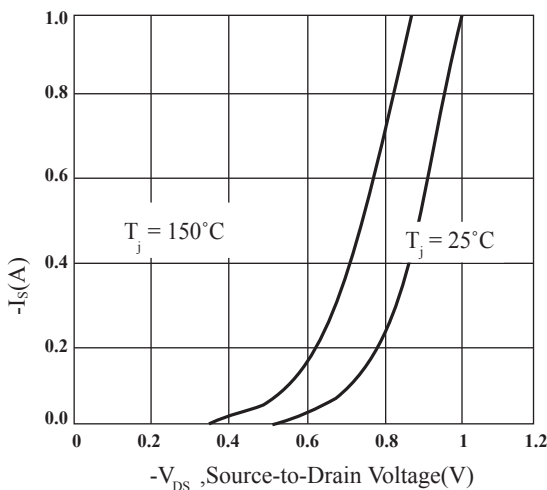


Fig.5 Forward Characteristics of Reverse Diode

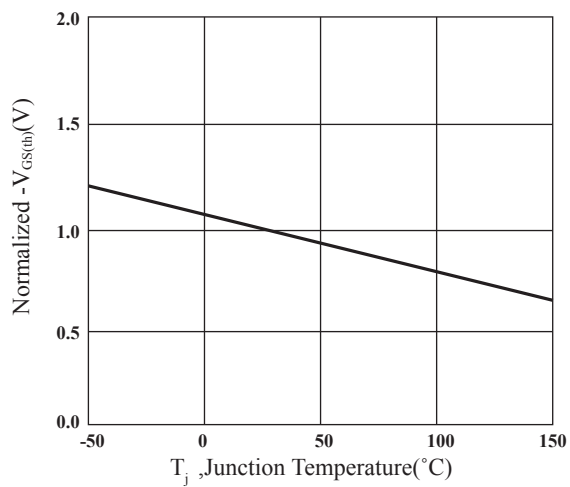


Fig.6 Gate Threshold Voltage v.s. Junction Temperature

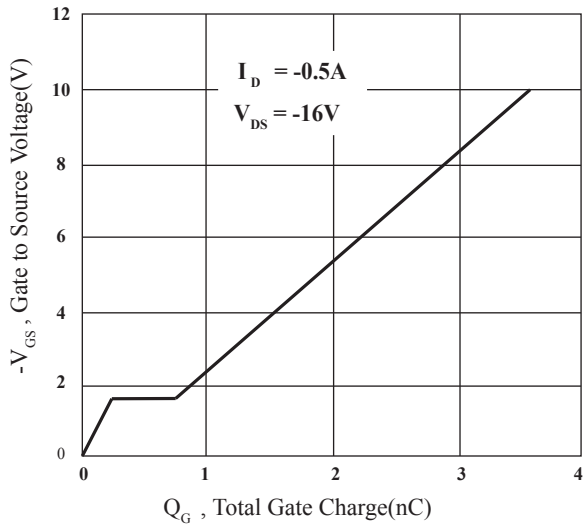


Fig 7. Gate Charge Characteristics

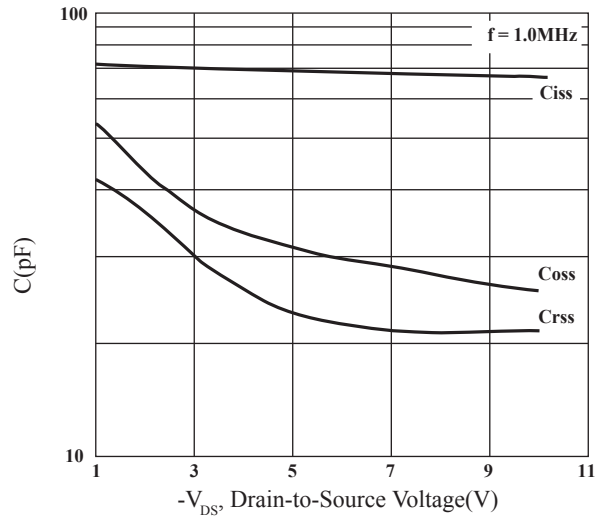


Fig 8. Typical Capacitance Characteristics

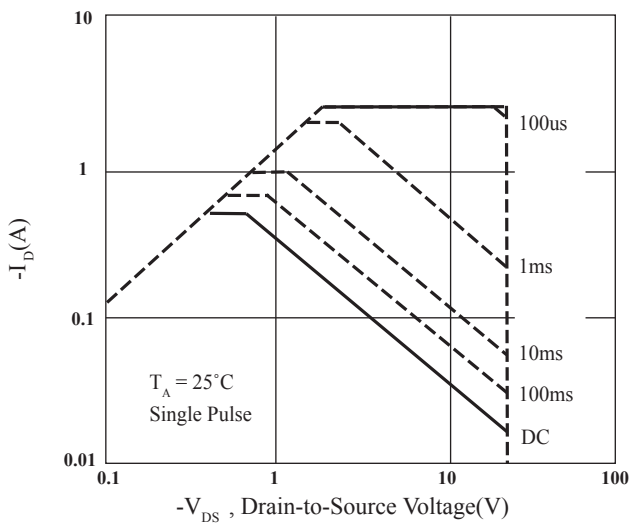


Fig 9. Maximum Safe Operation Area

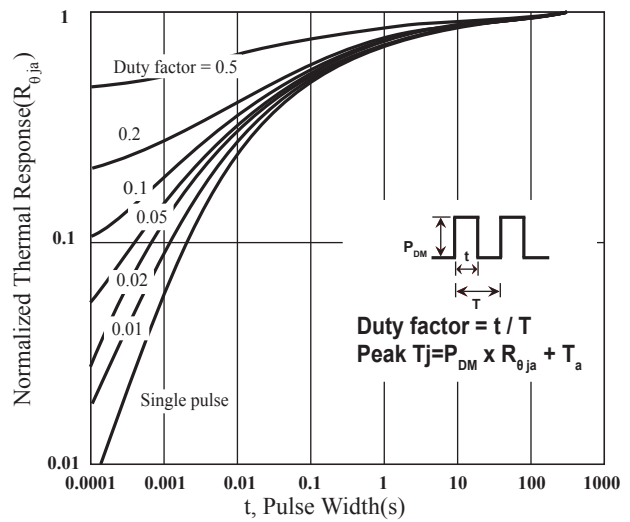


Fig 10. Effective Transient Thermal Impedance

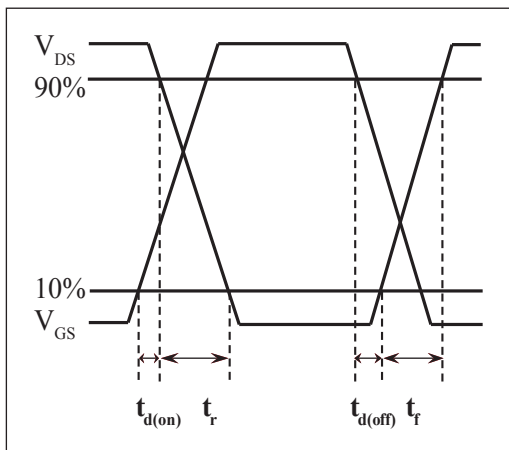


Fig 11. Switching Time Circuit

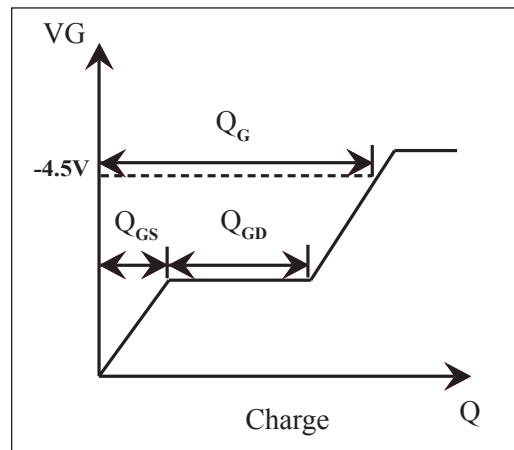


Fig 12. Gate Charge Waveform

SOT-23 Outline Dimension

Unit:mm

